	L #	Hits	Search Text	DBs
1	L1	770	(fold$3 compound double multiple) adj2 compare	USPAT; US-PGPUB
2	L2	7726	(fault trap exception) near20 (previous$3 earlier first compar$4) near10 (data value result)	USPAT; US-PGPUB
3	L3	18	1 and 2	USPAT; US-PGPUB
4	L7	44	(fault trap exception) near20 (data value result) and 1 not 3	USPAT; US-PGPUB
5	L4	31	((fold$3 compound double multiple) adj2 compare).ab,ti.	USPAT; US-PGPUB
6	L8	3	(fault trap exception) and 4 not (3 5 7)	USPAT; US-PGPUB
7	L5	2	(fault trap exception) near99 1	USPAT; US-PGPUB
8	L11	218	(fold$3 compound double multiple) adj2 compare	EPO; JPO; DERWENT; IBM_TDB
9	L12	1	(fault trap exception) near20 (operand data value result) and 11	EPO; JPO; DERWENT; IBM_TDB
10	L13	3	(fault trap exception) and 11	EPO; JPO; DERWENT; IBM_TDB
11	L14	47	(fault trap exception) near20 (operand data value result) and 1 not 3	USPAT; US-PGPUB
12	L19	1100	(exception trap$3 fault) near10 ((memory page cache access$3 fetch$3 load$3 read$3 second next subsequent later) near10 (location position line address data operand)) near20 ((previous$3 earlier first compar$4) near5 (data value operand result))	USPAT; US-PGPUB
13	L21	431	(exception trap$3 fault) near10 ((memory page cache access$3 fetch$3 load$3 read$3 second next subsequent later) near10 (location position line address data operand)) near20 ((previous$3 earlier first compar$4) near5 (data value operand result))	EPO; JPO; DERWENT; IBM_TDB
14	L24	7654	instruction near20 (vector simd (plural plurality multiple multiplicity several two second) adj5 (memory cache page access$3 read load$3 fetch$3 location position address line data operand))	EPO; JPO; DERWENT; IBM_TDB
15	L26	30524	instruction near20 (vector simd (plural plurality multiple multiplicity several two second) adj5 (memory cache page access$3 read load$3 fetch$3 location position address line data operand))	USPAT; US-PGPUB
16	L28	274	19 and 26	USPAT; US-PGPUB
17	L33	8	21 and 24	EPO; JPO; DERWENT; IBM_TDB

	L #	Hits	Search Text	DBs
1	L1	770	(fold$3 compound double multiple) adj2 compare	USPAT; US-PGPUB
2	L2	7726	(fault trap exception) near20 (previous$3 earlier first compar$4) near10 (data value result)	USPAT; US-PGPUB
3	L3	18	1 and 2	USPAT; US-PGPUB
4	L7	44	(fault trap exception) near20 (data value result) and 1 not 3	USPAT; US-PGPUB
5	L4	31	((fold$3 compound double multiple) adj2 compare).ab,ti.	USPAT; US-PGPUB
6	L8	3	(fault trap exception) and 4 not (3 5 7)	USPAT; US-PGPUB
7	L5	2	(fault trap exception) near99 1	USPAT; US-PGPUB
8	L11	218	(fold$3 compound double multiple) adj2 compare	EPO; JPO; DERWENT; IBM_TDB
9	L12	1	(fault trap exception) near20 (operand data value result) and 11	EPO; JPO; DERWENT; IBM_TDB
10	L13	3	(fault trap exception) and 11	EPO; JPO; DERWENT; IBM_TDB
11	L14	47	(fault trap exception) near20 (operand data value result) and 1 not 3	USPAT; US-PGPUB
12	L19	1100	(exception trap$3 fault) near10 ((memory page cache access$3 fetch$3 load$3 read$3 second next subsequent later) near10 (location position line address data operand)) near20 ((previous$3 earlier first compar$4) near5 (data value operand result))	USPAT; US-PGPUB
13	L21	431	(exception trap$3 fault) near10 ((memory page cache access$3 fetch$3 load$3 read$3 second next subsequent later) near10 (location position line address data operand)) near20 ((previous$3 earlier first compar$4) near5 (data value operand result))	EPO; JPO; DERWENT; IBM_TDB
14	L24	7654	instruction near20 (vector simd (plural plurality multiple multiplicity several two second) adj5 (memory cache page access$3 read load$3 fetch$3 location position address line data operand))	EPO; JPO; DERWENT; IBM_TDB
15	L26	30524	instruction near20 (vector simd (plural plurality multiple multiplicity several two second) adj5 (memory cache page access$3 read load$3 fetch$3 location position address line data operand))	USPAT; US-PGPUB
16	L28	274	19 and 26	USPAT; US-PGPUB
17	L30	8	21 and 24	EPO; JPO; DERWENT; IBM_TDB

	Document ID	U	Title	Current OR
1	US 20040054813 A1	☐	TCP offload network interface device	709/250
2	US 20040042293 A1	☒	Semiconductor memory and method of testing the same	365/202
3	US 20040030745 A1	☒	Method and apparatus for distributing network traffic processing on a multiprocessor computer	709/203
4	US 20040019774 A1	☒	Processor device and information processing device, compiling device, and compiling method using said processor device	712/244
5	US 20040019768 A1	☒	Method and system for using dynamic, deferred operation information to control eager deferral of control-speculative loads	712/216
6	US 20040019542 A1	☒	Timesheet reporting and extraction system and method	705/32
7	US 20040015680 A1	☒	Data processor for modifying and executing operation of instruction code	712/226
8	US 20040003126 A1	☒	TCP/IP offload network interface device	709/250
9	US 20040001008 A1	☒	Dynamic self-configuring metering network	340/870.02
10	US 20030204705 A1	☒	Prediction of branch instructions in a data processing apparatus	712/207
11	US 20030149578 A1	☒	Intelligent procurement agent	705/1
12	US 20030120974 A1	☒	Programable multi-port memory bist with compact microcode	714/31
13	US 20030097524 A1	☒	System, apparatus and method provding adaptive write policy for disk array controllers	711/114
14	US 20030063613 A1	☒	Label switched communication network and system and method for path restoration	370/401
15	US 20030061471 A1	☒	Data processor	712/226
16	US 20030043792 A1	☒	Label switched communication network, a method of conditioning the network and a method of data transmission	370/386
17	US 20030028746 A1	☒	Multiple address translations	711/206

	Document ID	U	Title	Current OR
18	US 20020199087 A1	☒	Configuration control within data processing systems	712/227
19	US 20020191538 A1	☒	Bi-directional line switched ring with uninterrupted service restoration	370/222
20	US 20020184477 A1	☒	Apparatus and method for facilitating debugging of sequences of processing instructions	712/227
21	US 20020184292 A1	☒	Method and apparatus for exception handling in a multi-processing environment	718/102
22	US 20020166113 A1	☒	Compiler generation of instruction sequences for unresolved storage references	717/140
23	US 20020161919 A1	☒	Fast-path processing for receiving data on TCP connection offload devices	709/238
24	US 20020156927 A1	☒	TCP/IP offload network interface device	709/250
25	US 20020154370 A1	☒	Optic relay unit and terminal station in light transmission system	398/177
26	US 20020147872 A1	☒	Sequentially performed compound compare-and-swap	710/200
27	US 20020147839 A1	☒	Fast-path apparatus for receiving data corresponding to a TCP connection	709/238
28	US 20020133692 A1	☒	Data processor	712/244
29	US 20020120830 A1	☒	Data processor assigning the same operation code to multiple operations	712/209
30	US 20020091844 A1	☒	Network interface device that fast-path processes solicited session layer read commands	709/230
31	US 20020087841 A1	☒	Circuit and method for supporting misaligned accesses in the presence of speculative load Instructions	712/225
32	US 20020087732 A1	☒	Transmit fast-path processing on TCP/IP offload network interface device	709/250
33	US 20020083243 A1	☒	Clustered computer system with deadlock avoidance	710/107
34	US 20020083149 A1	☒	Method for deadlock avoidance in a cluster environment	709/215

	Document ID	U	Title	Current OR
35	US 20020077782 A1	☒	Secured microcontroller architecture	702/185
36	US 20020059546 A1	☒	Method of generating a pattern for testing a logic circuit and apparatus for doing the same	714/738
37	US 20020044536 A1	☒	WIRELESS COMMUNICATION SYSTEM HAVING NETWORK CONTROLLER AND WIRELESS COMMUNICATION DEVICE CONNECTED TO DIGITAL COMMUNICATION LINE, AND METHOD OF CONTROLLING SAID SYSTEM	370/329
38	US 20020013889 A1	☒	Distributed shared memory system with variable granularity	711/203
39	US 20020002669 A1	☒	DATA PROCESSOR	712/244
40	US 20010042158 A1	☒	METHOD OF PERFORMING RELIABLE UPDATES IN A SYMMETRICALLY BLOCKED NONVOLATILE MEMORY HAVING A BIFURCATED STORAGE ARCHITECTURE	711/103
41	US 20010037406 A1	☒	Intelligent network storage interface system	709/250
42	US 20010037397 A1	☒	Intelligent network interface system and method for accelerated protocol processing	709/230
43	US 20010034827 A1	☒	Active load address buffer	712/225
44	US 20010027496 A1	☒	Passing a communication control block to a local device such that a message is processed on the device	709/250
45	US 20010023460 A1	☒	Passing a communication control block from host to a local device such that a message is processed on the device	709/250
46	US 20010016827 A1	☒	Methods and apparatus for electronically storing and retreiving value information on a portable card	705/14
47	US 20010010084 A1	☒	Memory fault diagnosis and data restoration method, and memory apparatus using the same	714/42
48	US 20010005882 A1	☒	CIRCUIT AND METHOD FOR INITIATING EXCEPTION ROUTINES USING IMPLICIT EXCEPTION CHECKING	712/244
49	US 20010004757 A1	☒	Processor and method of controlling the same	712/218
50	US 6701427 B1	☒	Data processing apparatus and method for processing floating point instructions	712/244
51	US 6694454 B1	☒	Stuck and transient fault diagnostic system	714/30
52	US 6681322 B1	☒	Method and apparatus for emulating an instruction set extension in a digital computer system	712/244

	Document ID	U	Title	Current OR
53	US 6665708 B1	☒	Coarse grained determination of data dependence between parallel executed jobs in an information processing system	709/215
54	US 6658480 B2	☒	Intelligent network interface system and method for accelerated protocol processing	709/239
55	US 6654914 B1	☒	Network fault isolation	714/43
56	US 6640315 B1	☒	Method and apparatus for enhancing instruction level parallelism	714/17
57	US 6631392 B1	☒	Method and apparatus for predicting floating-point exceptions	708/498
58	US 6629231 B1	☒	System and method for efficient register file conversion of denormal numbers between scalar and SIMD formats	712/1
59	US 6622269 B1	☒	Memory fault isolation apparatus and methods	714/718
60	US 6598122 B2	☒	Active load address buffer	711/126
61	US 6594785 B1	☒	System and method for fault handling and recovery in a multi-processing system having hardware resources shared between multiple partitions	714/48
62	US 6594752 B1	☒	Meta-address architecture for parallel, dynamically reconfigurable computing	712/43
63	US 6591355 B2	☒	Distributed shared memory system with variable granularity	711/202
64	US 6591302 B2	☒	Fast-path apparatus for receiving data corresponding to a TCP connection	709/230
65	US 6587636 B1	☒	Fiber optic errorless switching system	398/5
66	US 6581150 B1	☒	Apparatus and method for improved non-page fault loads and stores	711/201
67	US 6574709 B1	☒	System, apparatus, and method providing cache data mirroring to a data storage system	711/119
68	US 6543006 B1	☒	Method and apparatus for automatic undo support	714/19
69	US 6542990 B1	☒	Array access boundary check by executing BNDCHK instruction with comparison specifiers	712/227
70	US 6536008 B1	☒	Fault insertion method, boundary scan cells, and integrated circuit for use therewith	714/726
71	US 6519725 B1	☒	Diagnosis of RAMS using functional patterns	714/718
72	US 6510530 B1	☒	At-speed built-in self testing of multi-port compact sRAMs	714/30
73	US 6499117 B1	☒	Network fault information management system in which fault nodes are displayed in tree form	714/49
74	US 6484253 B1	☒	Data processor	712/212
75	US 6434620 B1	☒	TCP/IP offload network interface device	709/230

	Document ID	U	Title	Current OR
76	US 6427173 B1	☒	Intelligent network interfaced device and system for accelerated communication	709/238
77	US 6425039 B2	☒	Accessing exception handlers without translating the address	710/269
78	US 6415394 B1	☒	Method and circuit for analysis of the operation of a microcontroller using signature analysis during operation	714/30
79	US 6412081 B1	☒	System and method for providing a trap and patch function to low power, cost conscious, and space constrained applications	714/34
80	US 6412040 B2	☒	Method of performing reliable updates in a symmetrically blocked nonvolatile memory having a bifurcated storage architecture	711/103
81	US 6408383 B1	☒	Array access boundary check by executing BNDCHK instruction with comparison specifiers	712/227
82	US 6393487 B2	☒	Passing a communication control block to a local device such that a message is processed on the device	709/238
83	US 6389479 B1	☒	Intelligent network interface device and system for accelerated communication	709/243
84	US 6381686 B1	☒	Parallel processor comprising multiple sub-banks to which access requests are bypassed from a request queue when corresponding page faults are generated	711/203
85	US 6378067 B1	☒	Exception reporting architecture for SIMD-FP instructions	712/244
86	US 6374347 B1	☒	Register file backup queue	712/228
87	US 6360314 B1	☒	Data cache having store queue bypass for out-of-order instruction execution and method for same	712/219
88	US 6357033 B1	☒	Communication processing control apparatus and information processing system having the same	714/758
89	US 6334153 B1	☒	Passing a communication control block from host to a local device such that a message is processed on the device	709/230
90	US 6304958 B1	☒	Microcomputer having data execution units mounted thereon	712/229
91	US 6298436 B1	☒	Method and system for performing atomic memory accesses in a processor system	712/220
92	US 6289445 B1	☒	Circuit and method for initiating exception routines using implicit exception checking	712/244
93	US 6279128 B1	☒	Autonomous system for recognition of patterns formed by stored data during computer memory scrubbing	714/49
94	US 6275982 B1	☒	Method and device enabling a fixed program to be developed	717/168
95	US 6272612 B1	☒	Process for allocating memory in a multiprocessor data processing system	711/203
96	US 6269407 B1	☒	Method and system for data filtering within an object-oriented data	719/315
97	US 6266447 B1	☒	Methods and apparatus for electronically storing and retrieving value information on a portable card	705/14
98	US 6247060 B1	☒	Passing a communication control block from host to a local device such that a message is processed on the device	709/238

	Document ID	U	Title	Current OR
99	US 6226680 B1	☒	Intelligent network interface system method for protocol processing	709/230
100	US 6209081 B1	☒	Method and system for nonsequential instruction dispatch and execution in a superscalar processor system	712/215
101	US 6189093 B1	☒	System for initiating exception routine in response to memory access exception by storing exception information and exception bit within architectured register	712/244
102	US 6182206 B1	☒	Dynamically reconfigurable computing using a processing unit having changeable internal hardware organization	712/43
103	US 6119218 A	☒	Method and apparatus for prefetching data in a computer system	712/207
104	US 6105129 A	☒	Converting register data from a first format type to a second format type if a second type instruction consumes data produced by a first type instruction	712/222
105	US 6101580 A	☒	Apparatus and method for assisting exact garbage collection by using a stack cache of tag bits	711/132
106	US 6098089 A	☒	Generation isolation system and method for garbage collection	718/104
107	US 6088759 A	☒	Method of performing reliable updates in a symmetrically blocked nonvolatile memory having a bifurcated storage architecture	711/103
108	US 6085312 A	☒	Method and apparatus for handling imprecise exceptions	712/208
109	US 6071717 A	☒	Object code logic analysis and automated modification system and method	717/128
110	US 6058469 A	☒	System and method for dynamically reconfigurable computing using a processing unit having changeable internal hardware organization	712/43
111	US 6052774 A	☒	Apparatus and method for identifying exception routines indicated by instruction address issued with an instruction fetch command	712/200
112	US 6049866 A	☒	Method and system for an efficient user mode cache manipulation using a simulated instruction	712/227
113	US 6038561 A	☒	Single-chip data processor handling synchronous and asynchronous exceptions by branching from a first exception handler to a second exception handler	712/244
114	US 6032265 A	☒	Fault-tolerant computer system	714/9
115	US 6011908 A	☒	Gated store buffer for an advanced microprocessor	714/19
116	US 6009516 A	☒	Pipelined microprocessor with efficient self-modifying code detection and handling	712/244
117	US 6005502 A	☒	Method for reducing the number of bits needed for the representation of constant values in a data processing device	341/65
118	US 5996062 A	☒	Method and apparatus for controlling an instruction pipeline in a data processing system	712/215
119	US 5974538 A	☒	Method and apparatus for annotating operands in a computer system with source instruction identifiers	712/218
120	US 5966529 A	☒	Processor having auxiliary operand register file and complementary arrangements for non-disruptively performing adjunct execution	712/228
121	US 5958070 A	☒	Remote checkpoint memory system and protocol for fault-tolerant computer system	714/13

	Document ID	U	Title	Current OR
122	US 5951676 A	☒	Apparatus and method for direct loading of offset register during pointer load operation	712/225
123	US 5948095 A	☒	Method and apparatus for prefetching data in a computer system	712/200
124	US 5930495 A	☒	Method and system for processing a first instruction in a first processing environment in response to intiating processing of a second instruction in a emulation environment	703/26
125	US 5926832 A	☒	Method and apparatus for aliasing memory data in an advanced microprocessor	711/141
126	US 5924114 A	☒	Circular buffer with two different step sizes	711/110
127	US 5912906 A	☒	Method and apparatus for recovering from correctable ECC errors	714/763
128	US 5903739 A	☒	System and method for processing load instruction in accordance with "no-fault" processing facility including arrangement for preserving access fault indicia	712/216
129	US 5901001 A	☒	Data processor and method of processing data	712/212
130	US 5898882 A	☒	Method and system for enhanced instruction dispatch in a superscalar processor system utilizing independently accessed intermediate storage	712/23
131	US 5896526 A	☒	Programmable instruction trap system and method	712/227
132	US 5890189 A	☒	Memory management and protection system for virtual memory in computer system	711/100
133	US 5881616 A	☒	Register file backup queue	714/15
134	US 5845298 A	☒	Write barrier system and method for trapping garbage collection page boundary crossing pointer stores	707/206
135	US 5838894 A	☒	Logical, fail-functional, dual central processor units formed from three processor units	714/11
136	US 5812868 A	☒	Method and apparatus for selecting a register file in a data processing system	712/23
137	US 5812759 A	☒	Fault handling with loaded functions	714/57
138	US 5802337 A	☒	Method and apparatus for executing load instructions speculatively	712/216
139	US 5794062 A	☒	System and method for dynamically reconfigurable computing using a processing unit having changeable internal hardware organization	712/30
140	US 5790826 A	☒	Reduced register-dependency checking for paired-instruction dispatch in a superscalar processor with partial register writes	712/216
141	US 5790776 A	☒	Apparatus for detecting divergence between a pair of duplexed, synchronized processor elements	714/10
142	US 5768500 A	☒	Interrupt-based hardware support for profiling memory system performance	714/47
143	US 5764942 A	☒	Method and system for selective serialization of instruction processing in a superscalar processor system	712/214
144	US 5761413 A	☒	Fault containment system for multiprocessor with shared memory	714/49

	Document ID	U	Title	Current OR
145	US 5758051 A	☒	Method and apparatus for reordering memory operations in a processor	714/2
146	US 5751946 A	☒	Method and system for detecting bypass error conditions in a load/store unit of a superscalar processor	714/50
147	US 5748873 A	☒	Fault recovering system provided in highly reliable computer system having duplicated processors	714/11
148	US 5742794 A	☒	Emulation techniques for computer systems having mixed processor/software configurations	703/26
149	US 5736987 A	☒	Compression of graphic data normals	345/420
150	US 5726975 A	☒	Switching system capable of performing alternative routing in accordance with an alternative routing scenario assembled in a maintenance terminal	370/228
151	US 5712997 A	☒	System and method for processing load instruction in accordance with "no-fault " processing facility including arrangement for preserving access fault indicia	712/217
152	US 5710941 A	☒	System for substituting protected mode hard disk driver for real mode driver by trapping test transfers to verify matching geometric translation	710/14
153	US 5706460 A	☒	Variable architecture computer with vector parallel processor and using instructions with variable length fields	712/204
154	US 5706422 A	☒	Method of locating fault of communication system	714/4
155	US 5701502 A	☒	Isolating a central processing unit from the operating system controlling said unit and its associated hardware for interaction of the unit with data handling apparatus alien to the operating system	709/201
156	US 5699506 A	☒	Method and apparatus for fault testing a pipelined processor	714/37
157	US 5689513 A	☒	Data transmission system having a backup testing facility	714/712
158	US 5680568 A	☒	Instruction format with sequentially performable operand address extension modification	711/220
159	US 5644848 A	☒	Processor system including an index buffer circuit and a translation look-aside buffer control circuit for processor-to-processor interfacing	711/207
160	US 5636341 A	☒	Fault processing method and information processing system	714/13
161	US 5627987 A	☒	Memory management and protection system for virtual memory in computer system	711/200
162	US 5617553 A	☒	Computer system which switches bus protocols and controls the writing of a dirty page bit of an address translation buffer	711/206
163	US 5608867 A	☒	Debugging system using virtual storage means, a normal bus cycle and a debugging bus cycle	714/47
164	US 5600848 A	☒	Counterflow pipeline processor with instructions flowing in a first direction and instruction results flowing in the reverse direction	712/42
165	US 5574942 A	☒	Hybrid execution unit for complex microprocessor	712/23
166	US 5574922 A	☒	Processor with sequences of processor instructions for locked memory updates	712/220

	Document ID	U	Title	Current OR
167	US 5560036 A	☒	Data processing having incircuit emulation function	712/227
168	US 5559977 A	☒	Method and apparatus for executing floating point (FP) instruction pairs in a pipelined processor by stalling the following FP instructions in an execution stage	712/244
169	US 5546551 A	☒	Method and circuitry for saving and restoring status information in a pipelined computer	707/102
170	US 5542052 A	☒	Applying traps to a printed page specified in a page description language format	345/589
171	US 5537559 A	☒	Exception handling circuit and method	712/244
172	US 5504925 A	☒	Apparatus and method for implementing interrupts in pipelined processors	712/244
173	US 5502827 A	☒	Pipelined data processor for floating point and integer operation with exception handling	712/244
174	US 5491829 A	☒	Method and system for indexing the assignment of intermediate storage buffers in a superscalar processor system	712/23
175	US 5469552 A	☒	Pipelined data processor having combined operand fetch and execution stage to reduce number of pipeline stages and penalty associated with branch instructions	712/244
176	US 5465373 A	☒	Method and system for single cycle dispatch of multiple instructions in a superscalar processor system	712/215
177	US 5440757 A	☒	Data processor having multistage store buffer for processing exceptions	712/228
178	US 5438670 A	☒	Method of prechecking the validity of a write access request	711/3
179	US 5428624 A	☒	Fault injection using boundary scan	714/727
180	US 5404557 A	☒	Data processor with plural instruction execution parts for synchronized parallel processing and exception handling	712/23
181	US 5390310 A	☒	Memory management unit having cross-domain control	711/203
182	US 5388215 A	☒	Uncoupling a central processing unit from its associated hardware for interaction with data handling apparatus alien to the operating system controlling said unit and hardware	709/229
183	US 5386563 A	☒	Register substitution during exception processing	712/228
184	US 5369767 A	☒	Servicing interrupt requests in a data processing system without using the services of an operating system	710/264
185	US 5369749 A	☒	Method and apparatus for the direct transfer of information between application programs running on distinct processors without utilizing the services of one or both operating systems	718/104
186	US 5363497 A	☒	System for removing section of memory from first system and allocating to second system in a manner indiscernable to both operating systems	711/153
187	US 5349651 A	☒	System for translation of virtual to physical addresses by operating memory management processor for calculating location of physical address in memory concurrently with cache comparing virtual addresses for translation	711/207
188	US 5339408 A	☒	Method and apparatus for reducing checking costs in fault tolerant processors	714/11

	Document ID	U	Title	Current OR
189	US 5325517 A	☒	Fault tolerant data processing system	714/11
190	US 5297263 A	☒	Microprocessor with pipeline system having exception processing features	712/244
191	US 5295236 A	☒	Applying traps to a printed page specified in a page description language format	715/527
192	US 5283868 A	☒	Providing additional system characteristics to a data processing system through operations of an application program, transparently to the operating system	709/227
193	US 5276847 A	☒	Method for locking and unlocking a computer address	711/163
194	US 5276822 A	☒	System with enhanced execution of address-conflicting instructions using immediate data latch for holding immediate data of a preceding instruction	712/218
195	US 5263153 A	☒	Monitoring control flow in a microprocessor	714/51
196	US 5255367 A	☒	Fault tolerant, synchronized twin computer system with error checking of I/O communication	714/11
197	US 5233700 A	☒	Address translation device with an address translation buffer loaded with presence bits	711/207
198	US 5220669 A	☒	Linkage mechanism for program isolation	718/108
199	US 5214770 A	☒	System for flushing instruction-cache only when instruction-cache address and data-cache address are matched and the execution of a return-from-exception-or-interrupt command	711/123
200	US 5210834 A	☐	High speed transfer of instructions from a master to a slave processor	712/207

	L #	Hits	Search Text	DBs
1	L1	770	(fold$3 compound double multiple) adj2 compare	USPAT; US-PGPUB
2	L2	7726	(fault trap exception) near20 (previous$3 earlier first compar$4) near10 (data value result)	USPAT; US-PGPUB
3	L3	18	1 and 2	USPAT; US-PGPUB
4	L7	44	(fault trap exception) near20 (data value result) and 1 not 3	USPAT; US-PGPUB
5	L4	31	((fold$3 compound double multiple) adj2 compare).ab,ti.	USPAT; US-PGPUB
6	L8	3	(fault trap exception) and 4 not (3 5 7)	USPAT; US-PGPUB
7	L5	2	(fault trap exception) near99 1	USPAT; US-PGPUB
8	L11	218	(fold$3 compound double multiple) adj2 compare	EPO; JPO; DERWENT; IBM_TDB
9	L12	1	(fault trap exception) near20 (operand data value result) and 11	EPO; JPO; DERWENT; IBM_TDB
10	L13	3	(fault trap exception) and 11	EPO; JPO; DERWENT; IBM_TDB
11	L14	47	(fault trap exception) near20 (operand data value result) and 1 not 3	USPAT; US-PGPUB
12	L19	1100	(exception trap$3 fault) near10 ((memory page cache access$3 fetch$3 load$3 read$3 second next subsequent later) near10 (location position line address data operand)) near20 ((previous$3 earlier first compar$4) near5 (data value operand result))	USPAT; US-PGPUB
13	L21	431	(exception trap$3 fault) near10 ((memory page cache access$3 fetch$3 load$3 read$3 second next subsequent later) near10 (location position line address data operand)) near20 ((previous$3 earlier first compar$4) near5 (data value operand result))	EPO; JPO; DERWENT; IBM_TDB
14	L24	7654	instruction near20 (vector simd (plural plurality multiple multiplicity several two second) adj5 (memory cache page access$3 read load$3 fetch$3 location position address line data operand))	EPO; JPO; DERWENT; IBM_TDB
15	L26	30524	instruction near20 (vector simd (plural plurality multiple multiplicity several two second) adj5 (memory cache page access$3 read load$3 fetch$3 location position address line data operand))	USPAT; US-PGPUB
16	L28	274	19 and 26	USPAT; US-PGPUB
17	L33	8	21 and 24	EPO; JPO; DERWENT; IBM_TDB

	Document ID	U	Title	Current OR
1	US 20030174555 A1	☐	Novel method and structure for efficient data verification operation for non-volatile memories	365/200
2	US 20030123320 A1	☐	Synchronous dynamic random access memory device	365/233
3	US 20020147872 A1	☐	Sequentially performed compound compare-and-swap	710/200
4	US 20020126528 A1	☐	Novel method and structure for efficient data verification operation for non-volatile memories	365/185.04
5	US 20020057722 A1	☐	Recording/reproducing apparatus, and method of detecting state thereof	372/43
6	US 6665222 B2	☐	Synchronous dynamic random access memory device	365/203
7	US 6560143 B2	☐	Method and structure for efficient data verification operation for non-volatile memories	365/185.04
8	US 6512711 B1	☐	Synchronous dynamic random access memory device	365/203
9	US 6401229 B1	☐	System and method for data error recovery on optical media utilizing hierarchical recovery techniques	714/769
10	US 6373752 B1	☐	Synchronous dynamic random access memory device	365/189.05
11	US 6351404 B1	☐	Synchronous dynamic random access memory device	365/51
12	US 6282633 B1	☐	High data density RISC processor	712/208
13	US 6215709 B1	☐	Synchronous dynamic random access memory device	365/189.11
14	US 6212111 B1	☐	Synchronous dynamic random access memory device	365/200
15	US 6172935 B1	☐	Synchronous dynamic random access memory device	365/233
16	US 6128710 A	☐	Method utilizing a set of blocking-symbol resource-manipulation instructions for protecting the integrity of data in noncontiguous data objects of resources in a shared memory of a multiple processor computer system	711/152
17	US 5347190 A	☐	Magnetic bearing systems	310/90.5
18	US 4541094 A	☐	Self-checking computer circuitry	714/53

	Document ID	U	Title	Current OR
1	US 20020147872 A1	☐	Sequentially performed compound compare-and-swap	710/200
2	US 4359624 A	☒	Welding apparatus with automatic following of the joint to be welded	219/124.34

	Document ID	U	Title	Current OR
36	US 6125439 A	☐	Process of executing a method on a stack-based processor	712/202
37	US 6076141 A	☐	Look-up switch accelerator and method of operating same	711/108
38	US 6054426 A	☐	Optically active aliphatic alcohols and their use as perfuming ingredients	512/22
39	US 6026485 A	☐	Instruction folding for a stack-based machine	712/226
40	US 6021469 A	☐	Hardware virtual machine instruction processor	711/125
41	US 6003128 A	☐	Number of pipeline stages and loop length related counter differential based end-loop prediction	712/241
42	US 5572671 A	☐	Method for operating application software in a safety critical environment	714/47
43	US 4697233 A	☐	Partial duplication of pipelined stack with data integrity checking	711/169
44	US 4132614 A	☐	Etching by sputtering from an intermetallic target to form negative metallic ions which produce etching of a juxtaposed substrate	204/192.32

	Document ID	U	Title	Current OR
1	US 20030123320 A1	☐	Synchronous dynamic random access memory device	365/233
2	US 20030071207 A1	☒	Deconvolution method and apparatus for analyzing compounds	250/282
3	US 20020147872 A1	☒	Sequentially performed compound compare-and-swap	710/200
4	US 20020117615 A1	☒	Deconvolution method and apparatus for analyzing compounds	250/282
5	US 6665222 B2	☒	Synchronous dynamic random access memory device	365/203
6	US 6631369 B1	☒	Method and system for incremental web crawling	707/4
7	US 6623935 B2	☒	Deconvolution method and apparatus for analyzing compounds	435/7.1
8	US 6529930 B1	☒	Methods and apparatus for performing a signed saturation operation	708/552
9	US 6524803 B2	☒	Deconvolution method and apparatus for analyzing compounds	435/7.1
10	US 6512711 B1	☒	Synchronous dynamic random access memory device	365/203
11	US 6477639 B1	☒	Branch instruction mechanism for processor	712/237
12	US 6373752 B1	☒	Synchronous dynamic random access memory device	365/189.05
13	US 6356997 B1	☒	Emulating branch instruction of different instruction set in a mixed instruction stream in a dual mode system	712/237
14	US 6351404 B1	☒	Synchronous dynamic random access memory device	365/51
15	US 6223335 B1	☒	Platform independent double compare and swap operation	717/100
16	US 6215709 B1	☒	Synchronous dynamic random access memory device	365/189.11
17	US 6215389 B1	☒	Time-independent, event-based system for receiving and discriminating unique codes from multiple transmitters and method for doing the same	340/5.1
18	US 6212111 B1	☒	Synchronous dynamic random access memory device	365/200
19	US 6209087 B1	☒	Data processor with multiple compare extension instruction	712/300
20	US 6172935 B1	☒	Synchronous dynamic random access memory device	365/233
21	US 6144986 A	☒	System for sorting in a multiprocessor environment	709/201

	Document ID	U	Title	Current OR
22	US 61377 07 A	☒	Method and apparatus for simultaneously performing a plurality of compare operations in content addressable memory device	365/49
23	US 61287 10 A	☒	Method utilizing a set of blocking-symbol resource-manipulation instructions for protecting the integrity of data in noncontiguous data objects of resources in a shared memory of a multiple processor computer system	711/152
24	US 61187 67 A	☒	Interference control for CDMA networks using a plurality of narrow antenna beams and an estimation of the number of users/remote signals present	370/252
25	US 60322 53 A	☒	Data processor with multiple compare extension instruction	712/300
26	US 59419 95 A	☒	Reloading state analyzer	714/39
27	US 57377 54 A	☒	Cache memory which selects one of several blocks to update by digitally combining control bits in all the blocks	711/136
28	US 53294 89 A	☒	DRAM having exclusively enabled column buffer blocks	365/189 .05
29	US 50903 51 A	☒	Vessel hull construction and method	114/65R
30	US 50254 58 A	☒	Apparatus for decoding frames from a data link	375/365
31	US 46189 68 A	☐	Output compare system and method automatically controlilng multiple outputs in a data processor	377/39

	Document ID	U	Title	Current OR
1	US 20020 14787 2 A	☐	Compound compare-and-swap operation implementation method in distributed computer system, involves reserving memory locations addressed by compare-and-swap instructions based on fixed total order of memory locations	
2	US 51931 87 A	☐	Fast interrupt mechanism for multiprocessor system - uses set of registers to identify association among multiple processors and comparison matrix to select processors	
3	DE 37194 06 A	☐	Correcting errors in digital audio data - reading from magnetic tape by using double recording, comparison and two sets of test words	

	Document ID	U	Title	Current OR
1	US 20040 01551 0 A1	☐	Obstruction-free synchronization for shared data structures	707/101
2	US 20030 22962 0 A1	☐	Method for efficient processing of multi-state attributes	707/2
3	US 20030 21283 0 A1	☐	Communications system using rings architecture	709/251
4	US 20030 20463 6 A1	☐	Communications system using rings architecture	709/251
5	US 20030 20034 3 A1	☐	Communications system using rings architecture	709/251
6	US 20030 20034 2 A1	☐	Communications system using rings architecture	709/251
7	US 20030 20033 9 A1	☐	Communications system using rings architecture	709/250
8	US 20030 19607 6 A1	☐	Communications system using rings architecture	712/234
9	US 20030 19599 1 A1	☐	Communications system using rings architecture	709/251
10	US 20030 19599 0 A1	☐	Communications system using rings architecture	709/251
11	US 20030 19598 9 A1	☐	Communications system using rings architecture	709/251
12	US 20030 19504 6 A1	☐	Target shooting scoring and timing system	463/49
13	US 20030 19186 3 A1	☐	Communications system using rings architecture	709/251
14	US 20030 19186 2 A1	☐	Communications system using rings architecture	709/251
15	US 20030 19186 1 A1	☐	Communications system using rings architecture	709/251
16	US 20030 18994 0 A1	☐	Communications system using rings architecture	370/406
17	US 20030 18246 5 A1	☐	Lock-free implementation of dynamic-sized shared data structure	719/314

	Document ID	U	Title	Current OR
18	US 20030 18246 2 A1	☐	Value recycling facility for multithreaded computations	719/310
19	US 20030 17457 2 A1	☐	Non-blocking memory management mechanism for supporting dynamic-sized data structures	365/230 .03
20	US 20030 17225 7 A1	☐	Communications system using rings architecture	712/234
21	US 20030 17219 0 A1	☐	Communications system using rings architecture	709/251
22	US 20030 17218 9 A1	☐	Communications system using rings architecture	709/251
23	US 20030 16734 8 A1	☐	Communications system using rings architecture	709/251
24	US 20030 14008 5 A1	☐	Single-word lock-free reference counting	718/107
25	US 20030 09845 7 A1	☐	Scan testing system, method, and apparatus	257/48
26	US 20030 06500 8 A1	☐	Selective estrogen receptor modulators in combination with estrogens	514/311
27	US 20030 04051 0 A1	☐	Selective estrogen receptor modulators in combination with estrogens	514/177
28	US 20020 19817 9 A1	☐	Selective estrogen receptor modulators in combination with estrogens	514/102
29	US 20020 09127 8 A1	☐	Steroid derived antibiotics	552/9
30	US 20020 01992 8 A1	☐	Processing architecture having a compare capability	712/222
31	US 20020 01937 6 A1	☐	Steroid derived antibiotics	514/169
32	US 65325 31 B1	☐	Method frame storage using multiple memory circuits	712/202
33	US 64861 48 B2	☐	Steroid derived antibiotics	514/182
34	US 63507 38 B1	☐	Steroid derived antibiotics	514/182
35	US 61638 37 A	☐	Writing of instruction results produced by instruction execution circuits to result destinations	712/216

	Document ID	U	Title	Current OR
36	US 6125439 A	☐	Process of executing a method on a stack-based processor	712/202
37	US 6076141 A	☐	Look-up switch accelerator and method of operating same	711/108
38	US 6054426 A	☐	Optically active aliphatic alcohols and their use as perfuming ingredients	512/22
39	US 6026485 A	☐	Instruction folding for a stack-based machine	712/226
40	US 6021469 A	☐	Hardware virtual machine instruction processor	711/125
41	US 6003128 A	☐	Number of pipeline stages and loop length related counter differential based end-loop prediction	712/241
42	US 5666535 A	☒	Microprocessor and data flow microprocessor having vector operation function	718/104
43	US 5572671 A	☐	Method for operating application software in a safety critical environment	714/47
44	US 5404553 A	☒	Microprocessor and data flow microprocessor having vector operation function	712/25
45	US 5081572 A	☒	Manipulation of time-ordered lists and instructions therefor	711/163
46	US 4697233 A	☐	Partial duplication of pipelined stack with data integrity checking	711/169
47	US 4132614 A	☐	Etching by sputtering from an intermetallic target to form negative metallic ions which produce etching of a juxtaposed substrate	204/192.32

	L #	Hits	Search Text	DBs
1	L14	18430	(rais$3 signal$4 handl$3 cancel$4 invalid$5 valid$3 prevent$3 inhibit$3) near10 (exception trap$3 fault) near10 (memory read$3 page access$3 cache fetch$3 load$3 second location position line address data operand)	USPAT; US-PGPUB
2	L16	26203	instruction near20 ((plural plurality multiple multiplicity several two second) adj5 (memory cache page access$3 read load$3 fetch$3 location position address line data operand))	USPAT; US-PGPUB
3	L18	2105	14 near20 ((second previous earlier subsequent next first) near10 (memory cache page access$3 read load$3 fetch$3 location position address line data operand))	USPAT; US-PGPUB
4	L19	432	16 and 18	USPAT; US-PGPUB
5	L20	10866	(rais$3 signal$4 handl$3 cancel$4 invalid$5 valid$3 prevent$3 inhibit$3) near10 (exception trap$3 fault) near10 (memory read$3 page access$3 cache fetch$3 load$3 second location position line address data operand)	EPO; JPO; DERWENT; IBM_TDB
6	L21	447	20 near20 ((second previous earlier subsequent next first) near10 (memory cache page access$3 read load$3 fetch$3 location position address line data operand))	EPO; JPO; DERWENT; IBM_TDB
7	L22	6101	instruction near20 ((plural plurality multiple multiplicity several two second) adj5 (memory cache page access$3 read load$3 fetch$3 location position address line data operand))	EPO; JPO; DERWENT; IBM_TDB
8	L23	8	21 and 22	EPO; JPO; DERWENT; IBM_TDB

	Document ID	U	Title	Current OR
1	JP 04040 587 A	☐	PORTABLE ELECTRONIC EQUIPMENT	
2	WO 97131 98 A1	☐	SELF-MODIFYING CODE HANDLING SYSTEM	
3	EP 61419 3 A2	☐	Method and apparatus for detecting retention faults in memories.	
4	US 57747 09 A	☐	Exception handling method e.g. for MIPS microprocessor, microcontroller - involves setting first bit to second logic state and registering address of immediately previous executed instruction when immediately previous instruction is branching related instruction	
5	US 57648 84 A	☐	Procedure execution monitoring apparatus for multiprocessor computer system - monitors procedure during time between first and second exceptions which are raised when instruction address and address of instructions subsequent to branch instructions are reached	
6	EP 61419 3 A	☐	Integrated circuit memory retention fault detection - causing each memory bank to execute three test sequences, each sequence delayed to allow detection or bit pattern from previous sequence	
7	EP 42390 6 A	☐	Predicting and optimising bidirectional program branches - including nullify bit in branch instruction which controls whether or not spatially following instruction will be nullified	
8	EP 39975 7 A	☐	Paired instruction processor precise exception handling mechanism - has stages for memory and ALU operations, and data writing procedures respectively	

	Document ID	U	Title	Current OR
1	US 20040054876 A1	☐	Synchronising pipelines in a data processing apparatus	712/218
2	US 20040054872 A1	☒	High-performance, superscalar-based computer system with out-of-order intstruction execution	712/206
3	US 20040030912 A1	☒	Systems and methods for the prevention of unauthorized use and manipulation of digital content	713/200
4	US 20040019891 A1	☒	Method and apparatus for optimizing performance in a multi-processing system	718/102
5	US 20040019880 A1	☒	Write-through caching a java local variable within a register of a register bank	717/136
6	US 20040019774 A1	☒	Processor device and information processing device, compiling device, and compiling method using said processor device	712/244
7	US 20040019770 A1	☒	Optimization apparatus, compiler program, optimization method and recording medium	712/227
8	US 20040019768 A1	☒	Method and system for using dynamic, deferred operation information to control eager deferral of control-speculative loads	712/216
9	US 20030195715 A1	☒	Automatic test vector generation method, test method making use of the test vectors as automatically generated, chip manufacturing method and automatic test vector generation program	702/117
10	US 20030187904 A1	☒	Device virtualization and assignment of interconnect devices	718/1
11	US 20030182543 A1	☒	TRAINING LINE PREDICTOR FOR BRANCH TARGETS	712/237
12	US 20030167387 A1	☒	Vector transfer system generating address error exception when vector to be transferred does not start and end on same memory page	712/4
13	US 20030145251 A1	☒	Dynamic trap table interposition for efficient collection of trap statistics	714/35
14	US 20030135844 A1	☒	Bytecode program interpreter apparatus and method with pre-verification of data type restrictions and object initialization	717/126
15	US 20030135717 A1	☒	Method and apparatus for transferring vector data	712/222
16	US 20030120960 A1	☒	Power management using processor throttling emulation	713/320
17	US 20030105943 A1	☒	Mechanism for processing speclative LL and SC instructions in a pipelined processor	712/216

	Document ID	U	Title	Current OR
18	US 20030093654 A1	☒	Handling of load errors in computer processors	712/220
19	US 20030093579 A1	☒	Method and system for concurrent handler execution in an SMI and PMI-based dispatch-execution framework	719/318
20	US 20030079113 A1	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/205
21	US 20030070060 A1	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
22	US 20030063613 A1	☒	Label switched communication network and system and method for path restoration	370/401
23	US 20030056087 A1	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/207
24	US 20030056086 A1	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/207
25	US 20030046053 A1	☒	Logic simulation	703/15
26	US 20030028759 A1	☒	EXCEPTION HANDLING FOR SIMD FLOATING POINT-INSTRUCTIONS	712/244
27	US 20030023837 A1	☒	Register file backup queue	712/228
28	US 20020199087 A1	☒	Configuration control within data processing systems	712/227
29	US 20020184477 A1	☒	Apparatus and method for facilitating debugging of sequences of processing instructions	712/227
30	US 20020184292 A1	☒	Method and apparatus for exception handling in a multi-processing environment	718/102
31	US 20020169999 A1	☒	Placing exception throwing instructions in compiled code	714/26
32	US 20020166113 A1	☒	Compiler generation of instruction sequences for unresolved storage references	717/140
33	US 20020161989 A1	☒	Apparatus and method for storing instruction set information	712/227
34	US 20020156977 A1	☒	Virtual caching of regenerable data	711/118

	Document ID	U	Title	Current OR
35	US 20020156962 A1	☒	Microprocessor having improved memory management unit and cache memory	711/3
36	US 20020154370 A1	☒	Optic relay unit and terminal station in light transmission system	398/177
37	US 20020152259 A1	☒	Pre-committing instruction sequences	709/201
38	US 20020147872 A1	☒	Sequentially performed compound compare-and-swap	710/200
39	US 20020124160 A1	☒	Register file backup queue	712/228
40	US 20020101995 A1	☒	Microprocessor using asynchronous public key decryption processing	380/277
41	US 20020092002 A1	☒	Method and apparatus for preserving precise exceptions in binary translated code	717/137
42	US 20020091916 A1	☒	Embedded-DRAM-DSP architecture	712/228
43	US 20020087845 A1	☒	Embedded-DRAM-DSP architecture	712/228
44	US 20020087841 A1	☒	Circuit and method for supporting misaligned accesses in the presence of speculative load Instructions	712/225
45	US 20020087806 A1	☒	Cache coherence protocol engine and method for efficient processing of interleaved memory transactions in a multiprocessor system	711/141
46	US 20020073131 A1	☒	Unified exception handling for hierarchical multi-interrupt architectures	718/102
47	US 20020040451 A1	☒	Resource access control	714/42
48	US 20020040450 A1	☒	Multiple trap avoidance mechanism	714/8
49	US 20020040429 A1	☒	Embedded-DRAM-DSP architecture	712/228
50	US 20020040422 A1	☒	Resource access control for a processor	711/156
51	US 20020032719 A1	☒	Method and system of dynamic memory management	718/107

	Document ID	U	Title	Current OR
52	US 20020 02932 8 A1	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
53	US 20020 01988 7 A1	☒	Intercepting system API calls	719/328
54	US 20020 01690 3 A1	☒	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
55	US 20020 00266 9 A1	☒	DATA PROCESSOR	712/244
56	US 20010 05653 0 A1	☒	SYSTEM FOR HANDLING LOAD ERRORS HAVING SYMBOLIC ENTITY GENERATOR TO GENERATE SYMBOLIC ENTITY AND ALU TO PROPAGATE THE SYMBOLIC ENTITY	712/220
57	US 20010 05205 3 A1	☒	Stream processing unit for a multi-streaming processor	711/138
58	US 20010 03458 8 A1	☒	System and method for abstracting and visualizing a rout map	703/2
59	US 20010 02738 3 A1	☒	Method and apparatus to test an instruction sequence	702/188
60	US 20010 00797 0 A1	☒	Automatic test vector generation method, test method making use of the test vectors as automatically generated, chip manufacturing method and automatic test vector generation program	702/117
61	US 67049 23 B1	☒	System and method for pre-verification of stack usage in bytecode program loops	717/128
62	US 67014 27 B1	☒	Data processing apparatus and method for processing floating point instructions	712/244
63	US 66979 36 B2	☒	Register file backup queue	712/228
64	US 66657 49 B1	☒	Bus protocol for efficiently transferring vector data	710/29
65	US 66585 59 B1	☒	Method and apparatus for advancing load operations	712/245
66	US 66548 69 B1	☒	Assigning a group tag to an instruction group wherein the group tag is recorded in the completion table along with a single instruction address for the group to facilitate in exception handling	712/24
67	US 66511 32 B1	☒	System and method for emulating the operation of a translation look-aside buffer	711/6
68	US 66474 90 B2	☒	Training line predictor for branch targets	712/233
69	US 66474 85 B2	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
70	US 66369 59 B1	☒	Predictor miss decoder updating line predictor storing instruction fetch address and alignment information upon instruction decode termination condition	712/204

	Document ID	U	Title	Current OR
71	US 6631514 B1	☒	Emulation system that uses dynamic binary translation and permits the safe speculation of trapping operations	717/137
72	US 6631392 B1	☒	Method and apparatus for predicting floating-point exceptions	708/498
73	US 6629231 B1	☒	System and method for efficient register file conversion of denormal numbers between scalar and SIMD formats	712/1
74	US 6629207 B1	☒	Method for loading instructions or data into a locked way of a cache memory	711/125
75	US 6625726 B1	☒	Method and apparatus for fault handling in computer systems	712/245
76	US 6625720 B1	☒	System for posting vector synchronization instructions to vector instruction queue to separate vector instructions from different application programs	712/4
77	US 6622269 B1	☒	Memory fault isolation apparatus and methods	714/718
78	US 6622218 B2	☒	Cache coherence protocol engine and method for efficient processing of interleaved memory transactions in a multiprocessor system	711/141
79	US 6615300 B1	☒	Fast look-up of indirect branch destination in a dynamic translation system	710/100
80	US 6611779 B2	☒	Automatic test vector generation method, test method making use of the test vectors as automatically generated, chip manufacturing method and automatic test vector generation program	702/117
81	US 6604188 B1	☒	Pipeline replay support for multi-cycle operations wherein all VLIW instructions are flushed upon detection of a multi-cycle atom operation in a VLIW instruction	712/24
82	US 6598128 B1	☒	Microprocessor having improved memory management unit and cache memory	711/144
83	US 6594785 B1	☒	System and method for fault handling and recovery in a multi-processing system having hardware resources shared between multiple partitions	714/48
84	US 6594750 B1	☒	Method and apparatus for handling an accessed bit in a page table entry	711/207
85	US 6591340 B2	☒	Microprocessor having improved memory management unit and cache memory	711/118
86	US 6587636 B1	☒	Fiber optic errorless switching system	398/5
87	US 6581150 B1	☒	Apparatus and method for improved non-page fault loads and stores	711/201
88	US 6553486 B1	☒	Context switching for vector transfer unit	712/222
89	US 6553460 B1	☒	Microprocessor having improved memory management unit and cache memory	711/125
90	US 6549959 B1	☒	Detecting modification to computer memory by a DMA device	710/22
91	US 6546465 B1	☒	Integrating operating systems and run-time systems	717/114
92	US 6546478 B1	☒	Line predictor entry with location pointers and control information for corresponding instructions in a cache line	712/204

	Document ID	U	Title	Current OR
93	US 6543006 B1	☒	Method and apparatus for automatic undo support	714/19
94	US 6542988 B1	☒	Sending both a load instruction and retrieved data from a load buffer to an annex prior to forwarding the load data to register file	712/225
95	US 6536008 B1	☒	Fault insertion method, boundary scan cells, and integrated circuit for use therewith	714/726
96	US 6519694 B2	☒	System for handling load errors having symbolic entity generator to generate symbolic entity and ALU to propagate the symbolic entity	712/220
97	US 6513107 B1	☒	Vector transfer system generating address error exception when vector to be transferred does not start and end on same memory page	712/4
98	US 6505291 B1	☒	Processor having a datapath and control logic constituted with basis execution blocks	712/201
99	US 6496926 B1	☒	Computer-implemented paramaterless language with exception handler	712/245
100	US 6493116 B1	☒	PMD characterization across multiple optical channels of an optical link	398/20
101	US 6477702 B1	☒	Bytecode program interpreter apparatus and method with pre-verification of data type restrictions and object initialization	717/126
102	US 6442707 B1	☒	Alternate fault handler	714/10
103	US 6430657 B1	☒	COMPUTER SYSTEM THAT PROVIDES ATOMICITY BY USING A TLB TO INDICATE WHETHER AN EXPORTABLE INSTRUCTION SHOULD BE EXECUTED USING CACHE COHERENCY OR BY EXPORTING THE EXPORTABLE INSTRUCTION, AND EMULATES INSTRUCTIONS SPECIFYING A BUS LOCK	711/138
104	US 6425039 B2	☒	Accessing exception handlers without translating the address	710/269
105	US 6424989 B1	☒	Object-oriented transaction computing system	709/201
106	US 6412043 B1	☒	Microprocessor having improved memory management unit and cache memory	711/118
107	US 6397379 B1	☒	Recording in a program execution profile references to a memory-mapped active device	717/140
108	US 6385712 B1	☒	Method and apparatus for segregation of virtual address space	711/206
109	US 6381692 B1	☒	Pipelined asynchronous processing	712/244
110	US 6378067 B1	☒	Exception reporting architecture for SIMD-FP instructions	712/244
111	US 6374347 B1	☒	Register file backup queue	712/228
112	US 6360314 B1	☒	Data cache having store queue bypass for out-of-order instruction execution and method for same	712/219
113	US 6349297 B1	☒	Information processing system for directing information request from a particular user/application, and searching/forwarding/retrieving information from unknown and large number of information resources	707/4
114	US 6345351 B1	☒	Maintenance of speculative state of parallel executed jobs in an information processing system	711/203

	Document ID	U	Title	Current OR
115	US 6343341 B1	☒	Efficient access to variable-length data on a sequential access storage medium	711/111
116	US 6333931 B1	☒	Method and apparatus for interconnecting a circuit-switched telephony network and a packet-switched data network, and applications thereof	370/385
117	US 6329139 B1	☒	Automated sorting system for matrices with memory	435/6
118	US 6321326 B1	☒	Prefetch instruction specifying destination functional unit and read/write access mode	712/207
119	US 6304963 B1	☒	Handling exceptions occuring during processing of vector instructions	712/244
120	US 6289446 B1	☒	Exception handling utilizing call instruction with context information	712/244
121	US 6282633 B1	☒	High data density RISC processor	712/208
122	US 6282630 B1	☒	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
123	US 6279101 B1	☒	Instruction decoder/dispatch	712/215
124	US 6272619 B1	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/41
125	US 6260190 B1	☒	Unified compiler framework for control and data speculation with recovery code	717/156
126	US 6259639 B1	☒	Semiconductor integrated circuit device capable of repairing defective parts in a large-scale memory	365/201
127	US 6256720 B1	☒	High performance, superscalar-based computer system with out-of-order instruction execution	712/23
128	US 6253317 B1	☒	Method and apparatus for providing and handling traps	712/244
129	US 6247171 B1	☒	Bytecode program interpreter apparatus and method with pre-verification of a data type restrictions and object initialization	717/126
130	US 6246422 B1	☒	Efficient method for storing texture maps in multi-bank memory	345/552
131	US 6233590 B1	☒	Server apparatus for distributed communications supporting multiple user/application environment	715/500
132	US 6226687 B1	☒	Method and apparatus for maintaining an order of data packets	709/246
133	US 6219828 B1	☒	Method for using two copies of open firmware for self debug capability	717/129
134	US 6216222 B1	☒	Handling exceptions in a pipelined data processing apparatus	712/244
135	US 6216218 B1	☒	Processor having a datapath and control logic constituted with basis execution blocks	712/201
136	US 6209083 B1	☒	Processor having selectable exception handling modes	712/229
137	US 6202204 B1	☒	Comprehensive redundant load elimination for architectures supporting control and data speculation	717/151

	Document ID	U	Title	Current OR
138	US 6195744 B1	☒	Unified multi-function operation scheduler for out-of-order execution in a superscaler processor	712/215
139	US 6189093 B1	☒	System for initiating exception routine in response to memory access exception by storing exception information and exception bit within architectured register	712/244
140	US 6175916 B1	☒	Common-thread inter-process function calls invoked by jumps to invalid addresses	712/228
141	US 6161208 A	☒	Storage subsystem including an error correcting cache and means for performing memory to memory transfers	714/764
142	US 6141742 A	☒	Method for reducing number of bits used in storage of instruction address pointer values	711/220
143	US 6141635 A	☒	Method of diagnosing faults in an emulated computer system via a heterogeneous diagnostic program	703/22
144	US 6136274 A	☒	Matrices with memories in automated drug discovery and units therefor	422/102
145	US 6128723 A	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
146	US 6128787 A	☒	Fast fault detection circuitry for a microprocessor	710/305
147	US 6125443 A	☒	Interrupt processing system and method for information processing system of pipeline control type	712/244
148	US 6119218 A	☒	Method and apparatus for prefetching data in a computer system	712/207
149	US 6101594 A	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/41
150	US 6098089 A	☒	Generation isolation system and method for garbage collection	718/104
151	US 6094729 A	☒	Debug interface including a compact trace record storage	714/25
152	US 6092181 A	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/206
153	US 6088789 A	☒	Prefetch instruction specifying destination functional unit and read/write access mode	712/207
154	US 6079015 A	☒	Data processing system having selectable exception table relocation and method therefor	712/244
155	US 6075940 A	☒	System and method for pre-verification of stack usage in bytecode program loops	717/126
156	US 6073226 A	☒	System and method for minimizing page tables in virtual memory systems	711/203
157	US 6064815 A	☒	System and method for generating fix-up code facilitating avoidance of an exception of a predetermined type in a digital computer system	717/138
158	US RE36673 E	☒	Viceband data set	375/220
159	US 6052774 A	☒	Apparatus and method for identifying exception routines indicated by instruction address issued with an instruction fetch command	712/200
160	US 6049866 A	☒	Method and system for an efficient user mode cache manipulation using a simulated instruction	712/227

	Document ID	U	Title	Current OR
161	US 60386 61 A	☒	Single-chip data processor handling synchronous and asynchronous exceptions by branching from a first exception handler to a second exception handler	712/244
162	US 60386 54 A	☒	High performance, superscalar-based computer system with out-of-order instruction execution	712/23
163	US 60386 53 A	☒	High-performance superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
164	US 60354 22 A	☒	Data processing system for controlling execution of a debug function and method therefor	714/35
165	US 60265 01 A	☒	Data processing system for controlling execution of a debug function and method thereof	714/38
166	US 60095 16 A	☒	Pipelined microprocessor with efficient self-modifying code detection and handling	712/244
167	US 60092 61 A	☒	Preprocessing of stored target routines for emulating incompatible instructions on a target processor	703/26
168	US 60031 29 A	☒	System and method for handling interrupt and exception events in an asymmetric multiprocessor architecture	712/244
169	US 60031 23 A	☒	Memory system with global address translation	711/207
170	US 59997 31 A	☒	Bytecode program interpreter apparatus and method with pre-verification of data type restrictions and object initialization	717/126
171	US 59875 99 A	☒	Target instructions prefetch cache	712/238
172	US 59875 85 A	☒	One-chip microprocessor with error detection on the chip	712/1
173	US 59830 04 A	☒	Computer, memory, telephone, communications, and transportation system and methods	709/227
174	US 59789 02 A	☒	Debug interface including operating system access of a serial/parallel debug port	712/227
175	US 59665 30 A	☒	Structure and method for instruction boundary machine state restoration	712/244
176	US 59665 29 A	☒	Processor having auxiliary operand register file and complementary arrangements for non-disruptively performing adjunct execution	712/228
177	US 59648 93 A	☒	Data processing system for performing a trace function and method therefor	714/39
178	US 59637 37 A	☒	Interupt vectoring for trace exception facility in computer systems	712/244
179	US 59616 29 A	☒	High performance, superscalar-based computer system with out-of-order instruction execution	712/23
180	US 59502 21 A	☒	Variably-sized kernel memory stacks	711/100
181	US 59499 96 A	☒	Processor having a variable number of stages in a pipeline	712/244
182	US 59480 95 A	☒	Method and apparatus for prefetching data in a computer system	712/200
183	US 59304 95 A	☒	Method and system for processing a first instruction in a first processing environment in response to intiating processing of a second instruction in a emulation environment	703/26

	Document ID	U	Title	Current OR
184	US 5926832 A	☒	Method and apparatus for aliasing memory data in an advanced microprocessor	711/141
185	US 5920690 A	☒	Method and apparatus for providing access protection in an integrated circuit	713/200
186	US 5918005 A	☒	Apparatus region-based detection of interference among reordered memory operations in a processor	714/38
187	US 5913050 A	☒	Method and apparatus for providing address-size backward compatibility in a processor using segmented memory	711/213
188	US 5907860 A	☒	System and method of retiring store data from a write buffer	711/117
189	US 5907708 A	☒	System and method for facilitating avoidance of an exception of a predetermined type in a digital computer system by providing fix-up code for an instruction in response to detection of an exception condition resulting from execution thereof	712/244
190	US 5905881 A	☒	Delayed state writes for an instruction processor	712/219
191	US 5903918 A	☒	Program counter age bits	711/220
192	US 5903739 A	☒	System and method for processing load instruction in accordance with "no-fault" processing facility including arrangement for preserving access fault indicia	712/216
193	US 5898877 A	☒	Processor using special instruction set to enhance exception handling	710/260
194	US 5898627 A	☒	Semiconductor memory having redundant memory cell array	365/200
195	US 5890189 A	☒	Memory management and protection system for virtual memory in computer system	711/100
196	US 5887189 A	☒	Microcontroller system for performing operations of multiple microcontrollers	712/32
197	US 5884062 A	☒	Microprocessor with pipeline status integrity logic for handling multiple stage writeback exceptions	712/218
198	US 5884059 A	☒	Unified multi-function operation scheduler for out-of-order execution in a superscalar processor	712/215
199	US 5881262 A	☒	Method and apparatus for blocking execution of and storing load operations during their execution	712/216
200	US 5881261 A	☐	Processing system that rapidly indentifies first or second operations of selected types for execution	712/214

	Document ID	U	Title	Current OR
1	US 5898877 A	☐	Processor using special instruction set to enhance exception handling	710/260
2	US 5898627 A	☒	Semiconductor memory having redundant memory cell array	365/200
3	US 5890189 A	☒	Memory management and protection system for virtual memory in computer system	711/100
4	US 5887189 A	☒	Microcontroller system for performing operations of multiple microcontrollers	712/32
5	US 5884062 A	☒	Microprocessor with pipeline status integrity logic for handling multiple stage writeback exceptions	712/218
6	US 5884059 A	☒	Unified multi-function operation scheduler for out-of-order execution in a superscalar processor	712/215
7	US 5881262 A	☒	Method and apparatus for blocking execution of and storing load operations during their execution	712/216
8	US 5881261 A	☐	Processing system that rapidly indentifies first or second operations of selected types for execution	712/214
9	US 5881216 A	☒	Register file backup queue	714/15
10	US 5867712 A	☒	Single chip integrated circuit system architecture for document instruction set computing	717/127
11	US 5864877 A	☒	Apparatus and method for fast forwarding of table index (TI) bit for descriptor table selection	711/208
12	US 5854913 A	☒	Microprocessor with an architecture mode control capable of supporting extensions of two distinct instruction-set architectures	712/210
13	US 5845331 A	☒	Memory system including guarded pointers	711/163
14	US 5845298 A	☒	Write barrier system and method for trapping garbage collection page boundary crossing pointer stores	707/206
15	US 5845064 A	☒	Method for testing and verification of a CPU using a reference model	714/33
16	US 5832292 A	☒	High-performance superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
17	US 5832289 A	☒	System for estimating worst time duration required to execute procedure calls and looking ahead/preparing for the next stack operation of the forthcoming procedure calls	712/30
18	US 5826109 A	☒	Method and apparatus for performing multiple load operations to the same memory location in a computer system	710/39
19	US 5826073 A	☒	Self-modifying code handling system	712/226
20	US 5812810 A	☒	Instruction coding to support parallel execution of programs	712/216
21	US 5809271 A	☒	Method and apparatus for changing flow of control in a processor	712/208
22	US 5806068 A	☒	Document data processor for an object-oriented knowledge management system containing a personal database in communication with a packet processor	707/103 R
23	US 5799165 A	☒	Out-of-order processing that removes an issued operation from an execution pipeline upon determining that the operation would cause a lengthy pipeline delay	712/214

	Document ID	U	Title	Current OR
24	US 5790846 A	☒	Interrupt vectoring for instruction address breakpoint facility in computer systems	712/244
25	US 5778245 A	☒	Method and apparatus for dynamic allocation of multiple buffers in a processor	712/23
26	US 5771363 A	☒	Single-chip microcomputer having an expandable address area	712/200
27	US 5761413 A	☒	Fault containment system for multiprocessor with shared memory	714/49
28	US 5758168 A	☒	Interrupt vectoring for optionally architected facilities in computer systems	710/260
29	US 5752013 A	☒	Method and apparatus for providing precise fault tracing in a superscalar microprocessor	712/227
30	US 5751985 A	☒	Processor structure and method for tracking instruction status to maintain precise state	712/218
31	US 5751983 A	☒	Out-of-order processor with a memory subsystem which handles speculatively dispatched load operations	712/216
32	US 5745758 A	☒	System for regulating multicomputer data transfer by allocating time slot to designated processing task according to communication bandwidth capabilities and modifying time slots when bandwidth change	718/102
33	US 5745724 A	☒	Scan chain for rapidly identifying first or second objects of selected types in a sequential list	712/213
34	US 5742755 A	☒	Error-handling circuit and method for memory address alignment double fault	714/53
35	US 5740441 A	☒	Bytecode program interpreter apparatus and method with pre-verification of data type restrictions and object initialization	717/134
36	US 5740398 A	☒	Program order sequencing of data in a microprocessor with write buffer	711/117
37	US 5737516 A	☒	Data processing system for performing a debug function and method therefor	714/38
38	US 5729728 A	☒	Method and apparatus for predicting, clearing and redirecting unpredicted changes in instruction flow in a microprocessor	712/234
39	US 5726975 A	☒	Switching system capable of performing alternative routing in accordance with an alternative routing scenario assembled in a maintenance terminal	370/228
40	US 5724536 A	☒	Method and apparatus for blocking execution of and storing load operations during their execution	712/216
41	US 5721857 A	☒	Method and apparatus for saving the effective address of floating point memory operations in an out-of-order microprocessor	712/23
42	US 5717883 A	☒	Method and apparatus for parallel execution of computer programs using information providing for reconstruction of a logical sequential program	712/218
43	US 5717882 A	☒	Method and apparatus for dispatching and executing a load operation to memory	712/217
44	US 5713012 A	☒	Microprocessor	712/233
45	US 5712997 A	☒	System and method for processing load instruction in accordance with "no-fault " processing facility including arrangement for preserving access fault indicia	712/217

	Document ID	U	Title	Current OR
46	US 5706459 A	☒	Processor having a variable number of stages in a pipeline	712/200
47	US 5706422 A	☒	Method of locating fault of communication system	714/4
48	US 5704034 A	☒	Method and circuit for initializing a data processing system	714/38
49	US 5694574 A	☒	Method and apparatus for performing load operations in a computer system	711/140
50	US 5692170 A	☒	Apparatus for detecting and executing traps in a superscalar processor	712/244
51	US 5689720 A	☒	High-performance superscalar-based computer system with out-of-order instruction execution	712/23
52	US 5687344 A	☒	Single-chip microcomputer having an expandable address area	711/220
53	US 5687338 A	☒	Method and apparatus for maintaining a macro instruction for refetching in a pipelined processor	712/205
54	US 5684972 A	☒	Programmable servo burst sequencer for a disk drive	711/4
55	US 5673426 A	☒	Processor structure and method for tracking floating-point exceptions	712/244
56	US 5673408 A	☒	Processor structure and method for renamable trap-stack	712/216
57	US 5666508 A	☒	Four state two bit recoded alignment fault state circuit for microprocessor address misalignment fault generation	711/201
58	US 5664159 A	☒	Method for emulating multiple debug breakpoints by page partitioning using a single breakpoint register	703/23
59	US 5659721 A	☒	Processor structure and method for checkpointing instructions to maintain precise state	712/228
60	US 5655115 A	☒	Processor structure and method for watchpoint of plural simultaneous unresolved branch evaluation	712/239
61	US 5650996 A	☒	Method and apparatus for dynamic scheduling of instructions to ensure sequentially coherent data in a processor employing out-of-order execution	712/200
62	US 5651124 A	☒	Processor structure and method for aggressively scheduling long latency instructions including load/store instructions while maintaining precise state	712/215
63	US 5649136 A	☒	Processor structure and method for maintaining and restoring precise state at any instruction boundary	712/244
64	US 5644742 A	☒	Processor structure and method for a time-out checkpoint	712/244
65	US 5640583 A	☒	Programmable servo burst decoder	713/600
66	US 5640538 A	☒	Programmable timing mark sequencer for a disk drive	703/23
67	US 5636341 A	☒	Fault processing method and information processing system	714/13
68	US 5634027 A	☒	Cache memory system for multiple processors with collectively arranged cache tag memories	711/3

	Document ID	U	Title	Current OR
69	US 5630158 A	☒	Central processing unit including inhibited branch area	712/245
70	US 5627987 A	☒	Memory management and protection system for virtual memory in computer system	711/200
71	US 5624316 A	☒	Video game enhancer with intergral modem and smart card interface	463/45
72	US 5611064 A	☒	Virtual memory system	711/209
73	US 5603033 A	☒	Tool for debugging an operating system	717/124
74	US 5600848 A	☒	Counterflow pipeline processor with instructions flowing in a first direction and instruction results flowing in the reverse direction	712/42
75	US 5600844 A	☒	Single chip integrated circuit system architecture for document installation set computing	715/500
76	US 5598553 A	☒	Program watchpoint checking using paging with sub-page validity	703/23
77	US 5596717 A	☒	Four state token passing alignment fault state circuit for microprocessor address misalignment fault generation	714/53
78	US 5590312 A	☒	Method and apparatus for emulating circuitry in a computer system using a system management interrupt	703/23
79	US 5588113 A	☒	Register file backup queue	714/15
80	US 5584009 A	☒	System and method of retiring store data from a write buffer	711/117
81	US 5577200 A	☒	Method and apparatus for loading and storing misaligned data on an out-of-order execution computer system	714/50
82	US 5574922 A	☒	Processor with sequences of processor instructions for locked memory updates	712/220
83	US 5568380 A	☒	Shadow register file for instruction rollback	700/79
84	US 5560032 A	☒	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
85	US 5560013 A	☒	Method of using a target processor to execute programs of a source architecture that uses multiple address spaces	717/138
86	US 5559111 A	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
87	US 5537559 A	☒	Exception handling circuit and method	712/244
88	US 5526311 A	☒	Method and circuitry for enabling and permanently disabling test mode access in a flash memory device	365/201
89	US 5509130 A	☒	Method and apparatus for grouping multiple instructions, issuing grouped instructions simultaneously, and executing grouped instructions in a pipelined processor	712/215
90	US 5504925 A	☒	Apparatus and method for implementing interrupts in pipelined processors	712/244
91	US 5502827 A	☒	Pipelined data processor for floating point and integer operation with exception handling	712/244

	Document ID	U	Title	Current OR
92	US 5481685 A	☒	RISC microprocessor architecture implementing fast trap and exception state	712/244
93	US 5479618 A	☒	I/O module with reduced isolation circuitry	700/23
94	US 5471598 A	☒	Data dependency detection and handling in a microprocessor with write buffer	711/122
95	US 5469552 A	☒	Pipelined data processor having combined operand fetch and execution stage to reduce number of pipeline stages and penalty associated with branch instructions	712/244
96	US 5465376 A	☒	Microprocessor, coprocessor and data processing system using them	712/34
97	US 5450560 A	☒	Pointer for use with a buffer and method of operation	711/200
98	US 5450555 A	☒	Register logging in pipelined computer using register log queue of register content changes and base queue of register log queue pointers for respective instructions	712/228
99	US 5448705 A	☒	RISC microprocessor architecture implementing fast trap and exception state	712/244
100	US 5446876 A	☒	Hardware mechanism for instruction/data address tracing	714/47
101	US 5440757 A	☒	Data processor having multistage store buffer for processing exceptions	712/228
102	US 5440710 A	☒	Emulation of segment bounds checking using paging with sub-page validity	711/207
103	US 5440703 A	☒	System and method for saving state information in a multi-execution unit processor when interruptable instructions are identified	712/228
104	US 5438670 A	☒	Method of prechecking the validity of a write access request	711/3
105	US 5428624 A	☒	Fault injection using boundary scan	714/727
106	US 5426470 A	☒	Luminance and chrominance signal separation circuit employing comparison of level detected signal with a reference level	348/668
107	US 5423013 A	☒	System for addressing a very large memory with real or virtual addresses using address mode registers	711/163
108	US 5404557 A	☒	Data processor with plural instruction execution parts for synchronized parallel processing and exception handling	712/23
109	US 5404499 A	☒	Semi-automatic program execution error detection	714/54
110	US 5400321 A	☒	Central monitoring system of a multiplex subscriber loop carrier	370/248
111	US 5398330 A	☒	Register file backup queue	714/15
112	US 5390310 A	☒	Memory management unit having cross-domain control	711/203
113	US 5386563 A	☒	Register substitution during exception processing	712/228
114	US 5381419 A	☒	Method and apparatus for detecting retention faults in memories	714/720

	Document ID	U	Title	Current OR
115	US 5375213 A	☒	Address translation device and method for managing address information using the device	711/208
116	US 5361389 A	☒	Apparatus and method for emulation routine instruction issue	703/27
117	US 5361356 A	☒	Storage isolation with subspace-group facility	711/206
118	US 5349671 A	☒	Microprocessor system generating instruction fetch addresses at high speed	712/234
119	US 5349651 A	☒	System for translation of virtual to physical addresses by operating memory management processor for calculating location of physical address in memory concurrently with cache comparing virtual addresses for translation	711/207
120	US 5341482 A	☒	Method for synchronization of arithmetic exceptions in central processing units having pipelined execution units simultaneously executing instructions	712/244
121	US 5325299 A	☒	System for classifying lightning strikes to enhance location estimation thereof	702/4
122	US 5319553 A	☒	Lightning strike detection and mapping system with auto control of mapping display	702/4
123	US 5313647 A	☒	Digital data processor with improved checkpointing and forking	718/102
124	US 5309444 A	☒	Integrated circuit including a test cell for efficiently testing the accuracy of communication signals between a standard cell and an application cell	714/710
125	US 5305210 A	☒	Sampled data lightning strike detection and mapping system capable of early detection of an invalid strike from sampled data and quick resumption of monitoring an incoming signal	702/4
126	US 5303152 A	☒	Lightning strike detection system capable of quickly determining an invalid correlation of strike signaling	702/4
127	US 5299127 A	☒	Lightning strike detection and mapping system capable of monitoring its power source and of displaying a representation thereof on the mapping display	702/4
128	US 5297263 A	☒	Microprocessor with pipeline system having exception processing features	712/244
129	US 5295072 A	☒	Sampled data lightning strike detection and mapping system capable of recovering a pre threshold sample history for detection and mapping processing	702/4
130	US 5295071 A	☒	Sampled data lightning strike detection and mapping system capable of generating frequency spectrum of input signal waveforms and displaying such on the mapping display	702/4
131	US 5276848 A	☒	Shared two level cache including apparatus for maintaining storage consistency	711/121
132	US 5257358 A	☒	Method for counting the number of program instruction completed by a microprocessor	714/38
133	US 5237700 A	☒	Exception handling processor for handling first and second level exceptions with reduced exception latency	712/244
134	US 5233702 A	☒	Cache miss facility with stored sequences for data fetching	711/118
135	US 5233700 A	☒	Address translation device with an address translation buffer loaded with presence bits	711/207
136	US 5233698 A	☒	Method for operating data processors	713/601

	Document ID	U	Title	Current OR
137	US 5218711 A	☒	Microprocessor having program counter registers for its coprocessors	712/34
138	US 5210834 A	☒	High speed transfer of instructions from a master to a slave processor	712/207
139	US 5193181 A	☒	Recovery method and apparatus for a pipelined processing unit of a multiprocessor system	714/2
140	US 5140684 A	☒	Access privilege-checking apparatus and method	711/163
141	US 5119483 A	☒	Application of state silos for recovery from memory management exceptions	714/15
142	US 5113521 A	☒	Method and apparatus for handling faults of vector instructions causing memory management exceptions	714/15
143	US 5095426 A	☒	Data processing system for effectively handling exceptions during execution of two different types of instructions	712/244
144	US 5075844 A	☒	Paired instruction processor precise exception handling mechanism	712/218
145	US 5062041 A	☒	Processor/coprocessor interface apparatus including microinstruction clock synchronization	712/221
146	US 5043867 A	☒	Exception reporting mechanism for a vector processor	712/222
147	US 5008812 A	☒	Context switching method and apparatus for use in a vector processing system	712/228
148	US 4994961 A	☒	Coprocessor instruction format	710/110
149	US 4992934 A	☒	Reduced instruction set computing apparatus and methods	712/209
150	US 4985825 A	☒	System for delaying processing of memory access exceptions until the execution stage of an instruction pipeline of a virtual memory system based digital computer	711/169
151	US RE33280 E	☒	Voiceband data set	375/220
152	US 4959782 A	☒	Access arbitration for an input-output controller	710/240
153	US 4949250 A	☒	Method and apparatus for executing instructions for a vector processing system	712/208
154	US 4941241 A	☒	Microcomputer system including a master processor and a slave processor synchronized by three control lines	710/110
155	US 4916695 A	☒	Stored program controlled real time system including three substantially identical processors	714/11
156	US 4914578 A	☒	Method and apparatus for interrupting a coprocessor	710/260
157	US 4890253 A	☒	Predetermination of result conditions of decimal operations	708/525
158	US 4879676 A	☒	Method and apparatus for precise floating point exceptions	708/505
159	US 4875160 A	☒	Method for implementing synchronous pipeline exception recovery	712/228

	Document ID	U	Title	Current OR
160	US 4868738 A	☒	Operating system independent virtual memory computer system	710/26
161	US 4851990 A	☒	High performance processor interface between a single chip processor and off chip memory means having a dedicated and shared bus structure	710/100
162	US 4847748 A	☒	Virtual memory arrangement data processing system with decoding and execution of prefetched instructions in parallel	712/212
163	US 4841439 A	☒	Method for restarting execution interrupted due to page fault in a data processing system	712/244
164	US 4821231 A	☒	Method and apparatus for selectively evaluating an effective address for a coprocessor	710/110
165	US 4819154 A	☒	Memory back up system with one cache memory and two physically separated main memories	714/20
166	US 4811274 A	☒	Method and apparatus for selectively evaluating an effective address for a coprocessor	712/203
167	US 4809125 A	☒	Circuit interrupter apparatus with a style saving rating plug	361/93.3
168	US 4797816 A	☒	Virtual memory supported processor having restoration circuit for register recovering	711/220
169	US 4777593 A	☒	Vector processing apparatus including means for identifying the occurrence of exceptions in the processing of vector elements	712/9
170	US 4760518 A	☒	Bi-directional databus system for supporting superposition of vector and scalar operations in a computer	710/107
171	US 4758978 A	☒	Method and apparatus for selectively evaluating an effective address for a coprocessor	710/110
172	US 4758950 A	☒	Method and apparatus for selectively delaying an interrupt of a coprocessor	710/269
173	US 4757445 A	☒	Method and apparatus for validating prefetched instruction	712/207
174	US 4757440 A	☒	Pipelined data stack with access through-checking	714/53
175	US 4750110 A	☒	Method and apparatus for executing an instruction contingent upon a condition present in another data processor	710/110
176	US 4734865 A	☒	Insertion machine with audit trail and command protocol	700/222
177	US 4731736 A	☒	Method and apparatus for coordinating execution of an instruction by a selected coprocessor	710/110
178	US 4729094 A	☒	Method and apparatus for coordinating execution of an instruction by a coprocessor	712/34
179	US 4719565 A	☒	Interrupt and trap handling in microprogram sequencer	710/260
180	US 4710866 A	☒	Method and apparatus for validating prefetched instruction	712/207
181	US 4674032 A	☒	High-performance pipelined stack with over-write protection	711/169
182	US 4654819 A	☒	Memory back-up system	711/162

	Document ID	U	Title	Current OR
183	US 4648064 A	☒	Parallel process controller	710/45
184	US 4600986 A	☒	Pipelined split stack with high performance interleaved decode	711/169
185	US 4598364 A	☒	Efficient trace method adaptable to multiprocessors	714/38
186	US 4597041 A	☒	Method and apparatus for enhancing the operation of a data processing system	712/248
187	US 4591972 A	☒	Data processing system with unique microcode control	712/228
188	US 4590586 A	☒	Forced clear of a memory time-out to a maintenance exerciser	711/151
189	US 4569018 A	☒	Digital data processing system having dual-purpose scratchpad and address translation memory	711/207
190	US 4562536 A	☒	Directory test error mode control apparatus	714/25
191	US 4561088 A	☒	Communication system bypass architecture	370/222
192	US 4493027 A	☒	Method of performing a call operation in a digital data processing system having microcode call and return operations	712/228
193	US 4481573 A	☒	Shared virtual address translation unit for a multiprocessor system	711/207
194	US 4459664 A	☒	Multiprocessor computer system with dynamic allocation of multiprocessing tasks and processor for use in such multiprocessor computer system	718/105
195	US 4459661 A	☒	Channel address control system for a virtual machine system	718/100
196	US 4456952 A	☒	Data processing system having redundant control processors for fault detection	714/11
197	US 4455644 A	☒	Telecommunication fault detecting system	370/243
198	US 4419756 A	☒	Voiceband data set	379/93.32
199	US 4348721 A	☒	System for selectively addressing nested link return addresses in a microcontroller	712/243
200	US 4339797 A	☒	Microcontroller with auxiliary register for duplicating storage of data in one memory location	712/223